PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Whitman et al.

Serial No.: 09/944,230

Filed: August 30, 2001

For: SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

Confirmation No.: 2488

Examiner: T. Dickey

Group Art Unit: 2826

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/944,230 (hereinafter "the '230 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 010729, Frame No. 0057. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellants nor the undersigned attorney are aware of any action pending before the Board of Patent Appeals and Interferences (hereinafter "the Board") that would affect or influence the Board's decision in the above-referenced appeal.

III. STATUS OF CLAIMS

Claims 1-24 are currently pending in the above-referenced application.

Claims 2 and 5-10 have been withdrawn from consideration pursuant to an election made in response to a species election requirement.

Claims 1, 3, 4, and 11-24 have been considered.

Claims 1, 3, 4, 11-13, and 15-24 are subject to final rejections, which are under review in the above-referenced appeal.

Claim 14 has been objected to merely for depending from a base claim. The Examiner has indicated that the subject matter recited in claim 14 is allowable.

IV. STATUS OF AMENDMENTS

The '230 Application was filed on August 30, 2001, with twenty (20) claims.

A Preliminary Amendment, in which the specification and claims 4, 5, and 7 were amended, was mailed on December 26, 2001, and received a filing date of January 24, 2002.

On March 15, 2002, a species election requirement was made. In that requirement, the Examiner identified three species of invention. On March 21, 2002, a response was filed in which an election was made, without traverse, to prosecute claims that read on the stacked capacitor structure depicted in Figs. 2-4 of the above-referenced application. In responding to the species election requirement, it was noted that several claims remained generic to all three of the identified species of invention.

Evidently, on June 3, 2002, the Office mailed a first action on the merits of claims 1, 3, 4, and 11-20. That action was never received by the undersigned attorney.

On October 22, 2002, a Status Inquiry was mailed to the Office.

On January 24, 2003, the Office mailed a Notice of Abandonment. A Petition for Revival of an Application for Patent Abandoned Unavoidably was filed on January 30, 2003. On March 7, 2003, the Office mailed a Decision on the petition. The Office treated the Petition as a petition to withdraw a holding of abandonment, and withdrew the holding of abandonment. In view of its withdrawal of the holding of abandonment, the Office indicated that the Petition for Revival was moot. A copy of the June 3, 2002, Office Action was sent with the March 7, 2003, Decision.

An Amendment responsive to the June 3, 2002, Office Action was mailed with the appropriate certificate of mailing on Monday, June 9, 2003, and received a filing date of

June 13, 2004. In the Amendment, claims 4, 11, and 13 were revised, and explanations were provided as to the patentability of each of the claims that had been considered by the Examiner.

A second, non-final action was issued on July 30, 2003, in which several of the prior grounds for rejecting the claims had been withdrawn and replaced with new grounds of rejection. Additionally, in the action of July 30, 2003, the Examiner indicated that claim 14 is directed to allowable subject matter.

Another Amendment, which received a filing date of November 3, 2003, was filed in response to the second action. Formal revisions to each of claims 1-20, which did not alter the scopes of the claims, were presented in that Amendment. In addition, the new grounds for rejecting the claims were addressed, including reasoning as to why each of the claims that had been considered is allowable over the cited art.

On December 31, 2003, a Final Office Action was mailed. In the Final Office Action, the Examiner maintained all of the previously-presented claim rejections.

An Response to Final Office Action was filed on March 1, 2004. The Response presented additional reasoning as the patentability of the claims that had been considered.

On March 24, 2004, an Advisory Action followed.

A Request for Continued Examination ("RCE") was filed on April 30, 2004, with the appropriate petition and fee for extending the period for responding to the Final Office Action. An Amendment was filed with the RCE, revising claims 1 and 15 to remove unnecessary limitations and to improve the clarity with which the subject matter to which these claims are drawn is recited, and adding new claims 21-24. No further claim amendments have since been presented in the above-referenced application.

A non-final Office Action followed on June 16, 2004. The Examiner maintained his prior grounds for rejecting the claims that had been considered, and presented new grounds of rejection.

On September 21, 2004, another Response was filed. The Response included careful reasoning as to the allowability of claims 1-24 over the art upon which the Examiner has based his rejections.

The Examiner rejected this reasoning and, on November 3, 2004, issued another Final Office Action in the above-referenced application.

Explanations as to the patentability of claims 1-24 were again presented in a Response to Final Office Action dated January 3, 2005, which received a filing date of January 6, 2005, but the Examiner again rejected such reasoning, as evidenced by the Advisory Action and accompanying remarks dated January 27, 2005.

In view of the Examiner's continued and final rejection of the claims, a Notice of Appeal was filed on February 3, 2005, so that the final rejection could be reviewed. This Appeal Brief follows the Notice of Appeal. As April 3, 2005, fell on a Sunday and this Appeal Brief is being filed on Monday, April 4, 2005, it should be deemed to have been filed within two months of the filing date of the Notice of Appeal. 37 C.F.R. § 1.7.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims of the '230 Application are drawn to semiconductor device structures with material layers that at least partially fill recesses within the substrates of the semiconductor device structures and that are substantially free of hills and valleys. *See* independent claims 1

and 15. More specifically, the material layer of the semiconductor device structure recited in independent claim 1 *substantially fills* at least one recess in the substrate, while the material layer of the semiconductor device structure of independent claim 15 *at least partially fills* at least one recess in the substrate. The surfaces of these material layers may be free of abrasive planarization-induced defects (*see* claims 21 and 23), indicating that the substantially lack of hills or valleys in these surfaces may be achieved by means other than mechanical planarization or chemical-mechanical planarization techniques.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Claims 15-20, 23, and 24 are rejected under 35 U.S.C. § 102(e) for reciting subject matter that is purportedly anticipated by the subject matter disclosed in U.S. Patent 6,358,793 to Yates et al. (hereinafter "Yates");

(B) Claims 1, 3, 11-13, 21, and 22 have been rejected under 35 U.S.C. § 102(e) for being directed to subject matter which is assertedly anticipated by the subject matter described in U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi");

(C) Claims 1, 15, 16, and 21-24 stand rejected under 35 U.S.C. § 102(e) for being drawn to subject matter that is allegedly anticipated by the disclosure of U.S. Patent 6,461,932 to Wang (hereinafter "Wang");

(D) Claim 4 stands rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is allegedly unpatentable over teachings from Kikuchi, in view of the subject matter taught in U.S. Patent 5,663,090 to Dennison et al. (hereinafter "Dennison"); and

(E) Despite the fact that each of claims 1, 3, 4, and 15-20 remains generic to all of the species of invention that have been identified by the Examiner, the Examiner has not yet returned any of these claims to consideration, as M.P.E.P. § 806.04(d) requires when a generic claim is determined to be allowable.

VIII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102

Each of claims 1, 3, 11-13, and 15-24 stands rejected under 35 U.S.C. § 102(e).

1. LEGAL AUTHORITY

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

At page 7 of the Final Office Action, the Examiner incorrectly infers that, in order to for a claim to be allowable, the advantages of the subject matter recited therein must be clear. Advantages have not been described because such a description is not required by the law. Rather, the law states that a claim is patentable under 35 U.S.C. § 102 if the prior art does not expressly or inherently describe each and every element of that claim. Accordingly, the ensuing discussion, as required by the law, includes a characterization of the art upon which the Examiner

has relied, as well as an explanation as to why that art is deficient in expressly or inherently describing each and every element of the claims.

Although the Examiner has suggested otherwise by posing the question, "[a]re we not to trust the eyes," M.P.E.P. § 2125 cautions that "drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art." This rule is based, at least in part, upon the holding in *In re Aslanian,* 200 USPQ 500 (C.C.P.A. 1979), in which the court directed "[w]e evaluate and apply the teachings of all relevant references on the basis of what they reasonably disclose and suggested to one skilled in the art . . ." In *Aslanian,* the court was evaluating the relevance of drawings of a design patent as prior art to the claims of a utility patent application. Relative dimensions were not at issue. Therefore, it is apparent that reference to relative dimensions of features of an illustrated object in M.P.E.P. § 2125 is merely an example of something that may not be reasonably disclosed or suggested to one of ordinary skill in the art.

The C.C.P.A., in *In re Olson,* 101 USPQ 401 (1954), recognized that, unless expressly indicated, "drawings which accompany an application for a patent are merely illustrative of the principles embodied in the alleged invention claimed therein . . ." M.P.E.P. § 2125 provides further guidance on this principle by stating that illustrated drawing features are of little value in supporting a claim rejection when the specification does not indicate that the drawings may be relied upon for such a purpose.

2. REFERENCES RELIED UPON

Yates

Yates describes processes for forming localized masks within trenches that will be used to form capacitors. Such processes include, among other things, disposing a layer 40 of photoresist over the surface of a semiconductor device structure and within trenches that extend into an active surface thereof.

The Examiner has focused on the linear appearances of the upper surfaces of the photoresist layers 45, 70, 75 that are shown in the cross-sectional drawings of Yates (*e.g.*, FIGs. 11, 12, and 17) in support of its assertion that the surface of the photoresist layer 40 of Yates is free of hills and valleys.

Kikuchi

The description of Kikuchi is much like that of Yates. Specifically, FIG. 6D of Kikuchi shows a semiconductor device structure includes a substrate 21, multiple material layers 23-27 formed on the substrate 21, and a via-hole 23a extending downwardly into the material layers 23-27. *See also* FIGs. 6A-6C; col. 16, line 48, to col. 17, line 61. A resist 20 is then formed over the semiconductor device structure and within the via-holes 23a thereof. FIG. 6D; col. 17, line 62, to col. 18, line 2.

Wang

Wang describes a process for creating a trench-isolated semiconductor structure "using a pre-smoothing technique to avoid difficulties such as dishing and premature silicon-nitride

removal that might otherwise occur during chemical-mechanical polishing..." (hereinafter "CMP"). Col. 4, lines 48-51. While the avoidance of dishing a premature silicon nitride removal may prevent some of the nonplanarities that might occur during CMP, other types of nonplanarities may remain.

The process of Wang includes providing a dielectric layer 56 over a semiconductor surface, and covering the dielectric layer 56 with a "smoothening layer" 60. Col. 6, lines 23-28. The smoothening layer 60 has an upper smoothening surface 62 which is smoother than the upper dielectric surface 58 of the dielectric layer 56. Col. 6, lines 29-31. The smoothening layer 60 is applied either by a "deposition/spinning procedure" (col. 6, line 52, to col.7, line 14), a "deposition/flow" procedure (col. 7, lines 15-27), or a combination of these procedures (col. 7, lines 28-41). Wang notes, at col. 6, lines 32-34, that the smoothening layer 60 may include "slight depressions in upper smoothening surface 62 at the location so of the deepest parts of the depressed portion of upper dielectric surface 58."

Once the smoothening layer 60 has been formed, the smoothening layer 60 and the dielectric layer 56 are removed by CMP methods until a portion of the underlying semiconductor device is exposed. Col. 7, line 42, to col. 8, line 25.

3. ANALYSIS

a. YATES

Claims 15-20, 23, and 24 are rejected under 35 U.S.C. § 102(e) for reciting subject matter that is purportedly anticipated by the subject matter disclosed in Yates.

While Yates's figures depict an edge of an upper surface of the photoresist layer 40, at the depicted cross-section of the semiconductor device structure, as being substantially linear, the description of Yates is silent as to whether or not the upper surface of the photoresist layer 40 is actually "substantially free of hills and valleys," as recited in independent claim 15.

Moreover, it is notable that the straight lines that are shown in Yates do not represent any of the area of the surfaces of the depicted photoresist layers 45, 70, 75 but, rather, merely the edges of a surface of a cross-sectional plane that extends through photoresist layers 45, 70, 75 (*i.e.,* a single line across the surface of each photoresist layer 45, 70, 75). Before the priority date for the above-referenced application, one of ordinary skill in the art would have had no reason to believe or expect that such a straight line was representative of a planar surface. This is because, as is explained in the "Background" section of the above-referenced application and several of the references that have been made of record in the above-referenced application (*see, e.g.,* U.S. Patent 5,677,001 to Wang et al. (hereinafter "Wang '001"), col. 4, TABLE 1; U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara"), one of ordinary skill in the art would have expected the surface of a prior photoresist layer, particularly a photoresist layer which overlies a nonplanar substrate surface, to have a variety of miniscule nonplanar features, including hills and valleys of different elevations and dimensions, angled surfaces between the hills and valleys, and the like. As those of ordinary skill in the art have recognized, such surfaces have primarily been illustrated as planar for the sake of simplicity (*see, e.g.,* Wang '001 and Yoshihara).

In view of the guidance that has been provided in M.P.E.P. § 2125, without further guidance from the specification of Yates, the mere inclusion of straight lines in the simplified

drawings thereof does not indicate that the surface of photoresist layer 40, which is represented by a straight line, is substantially free of hills or valleys.

Thus, Yates does not expressly or inherently describe that the surfaces of any of the photoresist layers (*e.g.*, layers 45, 70, and 75 shown in FIGs. 17, 11, and 12, respectively) thereof have surfaces which are substantially free of hills or valleys, as required of the material layer of the semiconductor device structure recited in independent claim 15 of the above-referenced application. Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(e), Yates does not anticipate each and every element of independent claim 15 and, thus, that independent claim 15 recites subject matter which is allowable over the description of Yates.

Each of claims 16-20, 23, and 24 is allowable, among other reasons, for depending either directly or indirectly from claim 15, which is allowable.

Claim 20 is further allowable since Yates neither expressly nor inherently describes a material layer (*i.e.*, either the photoresist layer or the resulting mask layer thereof) that has a thickness which is less than the depths of the containers thereof. The relative dimensions shown in the drawings of Yates cannot be relied upon since Yates does "not disclose that the drawings are to scale and is silent as to dimensions." M.P.E.P. § 2125.

Claim 24 is additionally allowable since Yates lacks any express or inherent description that the surface of photoresist layer is substantially planar.

b. KIKUCHI

Claims 1, 3, 11-13, 21, and 22 have been rejected under 35 U.S.C. § 102(e) for being directed to subject matter which is assertedly anticipated by the subject matter described in Kikuchi.

The specification of Kikuchi does not expressly or inherently describe that a surface of the resist 20 is substantially free of hills or valleys, as is required of the material layer of the semiconductor device structure to which independent claim 1 is drawn. Again, it is respectfully submitted that, in view of the guidance provided by M.P.E.P. § 2125, reliance upon the drawings of Kikuchi is improper, since the specification does not indicate that the features (*e.g.*, straight lines) of the simplified drawings are to be taken at face value.

In contrast to the subject matter described in Kikuchi, independent claim 1 recites a semiconductor device structure which includes a material layer disposed over a substrate, substantially filling at least one recess of the substrate, and having a surface which is substantially free of hills and valleys.

Kikuchi is devoid of any express or inherent description that the resist layer 20 or any other layer described therein has a surface which is substantially free of hills and valleys. Moreover, Kikuchi repeatedly notes that the photoresist layers and other polymer layers disclosed therein have thicknesses of 10 μm. As "10 μm" denotes a layer of uniform thickness, and since the photoresist and other polymer layers of Kikuchi overlie nonplanar surfaces, none of these layers could be substantially free of hills and valleys.

It is, therefore, respectfully submitted that independent claim 1 recites subject matter which, under 35 U.S.C. § 102(e), is unanticipated by and allowable over the description of Kikuchi.

Each of claims 3, 11-13, 21, and 22 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 13 is additionally allowable since Kikuchi neither expressly nor inherently describes a mask material that has a thickness which is less than a depth of at least one container recessed in an insulator layer of the structure. Specifically, Kikuchi does not expressly or inherently describe that either the resist layer or the resulting mask layer of the structure disclosed therein has a thickness which is less than the depths of the via-holes 23a within which the resist is disposed. M.P.E.P. § 2125 clearly indicates that the relative dimensions shown in the drawings of Kikuchi cannot be relied upon since Kikuchi does "not disclose that the drawings are to scale and is silent as to dimensions."

Claim 24 is additionally allowable since Kikuchi lacks any express or inherent description that the surface of photoresist layer is substantially planar.

c. WANG

Claims 1, 15, 16, and 21-24 stand rejected under 35 U.S.C. § 102(e) for being drawn to subject matter that is allegedly anticipated by the disclosure of Wang.

Again, independent claims 1 and 15 require a material layer with a surface that is substantially free of both hills *and* valleys. As Wang teaches that the upper smoothening surface 62 of the smoothening layer 60 thereof may include "slight depressions" (*i.e.,* valleys),

Wang does not expressly or inherently describe a layer that is substantially free of both hills and *valleys*, as would be necessary to anticipate each and every element of independent claim 1 and independent claim 15. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), independent claims 1 and 15 recite subject matter which is allowable over the subject matter described in Wang.

Claims 21 and 22 are both allowable, among other reasons, for depending directly from claim 1, which is allowable.

Claims 16, 22, and 23 are each allowable, among other reasons, for depending directly from claim 15, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 3, 11-13, and 15-24 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claim 4 stands rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is allegedly unpatentable over teachings from Kikuchi, in view of the subject matter taught in Dennison.

Claim 4 is allowable, among other reasons, for depending from claims 1 and 3, which are allowable. Accordingly, reversal of the 35 U.S.C. § 103(a) rejection of claim 4 is respectfully requested.

C. SPECIES ELECTION REQUIREMENT

As each of claims 1, 3, 4, and 15-20 remains generic to all of the species of invention that have been identified by the Office, it is respectfully requested that claims 2 and 5-10 be returned to consideration and allowed. M.P.E.P. § 806.04(d).

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

It is respectfully submitted that:

(A) Claims 15-20, 23, and 24 recite subject matter that, under 35 U.S.C. § 102(e), is allowable over the subject matter disclosed in Yates;

(B) Under 35 U.S.C. § 102(e), the subject matter to which claims 1, 3, 11-13, 21, and 22 are drawn is allowable over the subject matter described in Kikuchi;

(C) Claims 1, 15, 16, and 21-24 are directed to subject matter that, under 35 U.S.C. § 102(e), is allowable over the disclosure of Wang;

(D) Claim 4 is allowable under 35 U.S.C. § 103(a) for being directed to subject matter which is patentable over teachings from Kikuchi, in view of the subject matter taught in Dennison; and

(E) In view of the allowability of claims 1, 3, 4, and 15-20, which remain generic to all of the species of invention that have been identified by the Examiner, claims 2 and 5-10 should be returned to consideration and allowed, as required by M.P.E.P. § 806.04(d).

In view of the foregoing, the rejections of claims 1, 3, 4, and 11-24 should be reversed, claims 2 and 5-10 should be returned to consideration, and each of these claims should be allowed.

Respectfully submitted,

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CLAIMS APPENDIX

1. A semiconductor device structure, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed over the substrate and substantially filling the at least one recess, the material layer having a surface substantially free of hills and valleys.

2. The semiconductor device structure of claim 1, wherein the substrate comprises a semiconductor substrate with a surface and the at least one recess comprises at least one trench recessed in the surface of the semiconductor substrate.

3. The semiconductor device structure of claim 1, wherein the material layer comprises a mask material.

4. The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess.

5. The semiconductor device structure of claim 1, wherein the substrate comprises:

a shallow trench isolation structure including a semiconductor device substrate with a surface and at least one trench formed in the surface of the semiconductor device substrate; and

an insulator layer substantially filling the at least one trench and covering the surface of the semiconductor device substrate.

6. The semiconductor device structure of claim 5, wherein the insulator layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device substrate and at least one valley located substantially above the at least one trench.

7. The semiconductor device structure of claim 6, wherein the material layer comprises a stress buffer layer that substantially fills the at least one valley in the insulator layer.

8. The semiconductor device structure of claim 1, wherein the substrate comprises:

a semiconductor device structure including a surface with at least one dual damascene trench formed thereon; and

a conductive layer substantially filling the at least one dual damascene trench and covering the surface of the semiconductor device structure.

9. The semiconductor device structure of claim 8, wherein the conductive layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device structure and at least one valley located substantially above the at least one dual damascene trench.

10. The semiconductor device structure of claim 9, wherein the material layer comprises a stress buffer layer that substantially fills the at least one valley in the conductive layer.

11. The semiconductor device structure of claim 1, wherein the substrate comprises a stacked capacitor structure and the at least one recess comprises at least one container recessed in an insulator layer of the stacked capacitor structure.

12. The semiconductor device structure of claim 11, wherein the material layer comprises a mask material, the mask material substantially filling the at least one container.

13. The semiconductor device structure of claim 12, wherein mask material covering a surface of the insulator layer has a thickness of less than a depth of the at least one container.

14. The semiconductor device structure of claim 12, wherein mask material covering a surface of the insulator layer has a thickness of less than about half a depth of the at least one container.

15. A semiconductor device structure, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed at least partially over the substrate so as to at least partially fill the at least one recess, the material layer having a surface substantially free of hills and valleys.

16. The semiconductor device structure of claim 15, wherein at least one region of the substrate is exposed through the material layer.

17. The semiconductor device structure of claim 15, further comprising:

at least one intermediate layer between the substrate and the material layer, at least one portion of the at least one intermediate layer at least partially filling the at least one recess.

18. The semiconductor device structure of claim 17, wherein at least one region of the at least one intermediate layer is exposed through the material layer.

19. The semiconductor device structure of claim 17, wherein the at least one intermediate layer comprises at least one of a mask material, an insulative material, and a conductive material.

20. The semiconductor device structure of claim 15, wherein the material layer has a thickness that is less than a depth of the at least one recess.

21. The semiconductor device structure of claim 1, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

22. The semiconductor device structure of claim 1, wherein the surface of the material layer is substantially planar.

23. The semiconductor device structure of claim 15, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

24. The semiconductor device structure of claim 15, wherein the surface of the material layer is substantially planar.